

Development of High Efficiency, Radiation Tolerant, Thin Silicon

Solar Cell

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prepared by

John Scott-Monck, Charles Gay and Paul Stella

of

Spectrolab, Inc.

12500 Gladstone Avenue

Sylmar, California 91342

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ABSTRACT

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Comparisons between polished and textured surface silicon solar cells indicate a gain in output averaging nearly seven percent for the textured surface cells, with thin cells (0.1mm) in some cases showing gains in excess of ten percent. Textured two ohm-cm cells 0.05mm thick have been produced which yield $\sim 14.5 \text{ mW/cm}^2$ under AMO conditions (10.7 percent efficiency). Optimized back surface field cells with AMO efficiencies as high as 15 percent have been made using two ohm-cm material 0.15mm (.006") in thickness.

↓ ↑

AMO 14.5 mW/cm²

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1.0 Summary

A sixteen element matrix of cells composed of polished and textured surface devices of various thicknesses and bulk resistivities was fabricated and delivered to JPL for evaluation. An optimized diffusion schedule for textured surface two and ten ohm-cm silicon cells was developed. Work was initiated to investigate methods for obtaining a reliable back surface field effect employing aluminum. This effort showed that an aluminum paste process in which the aluminum source was screen printed onto the wafers gave consistent results and demonstrated a superior back surface field effect when compared to the normal technique of vacuum evaporating the aluminum source.

Process technology for fabricating very thin (.05mm) silicon cells with textured surfaces was examined. Cells as thin as .045mm (1.8 mils) were successfully produced using textured two ohm-cm silicon. Approximately thirty cells ranging in thickness from .045 to .075mm have been made to date and power outputs of $\sim 14.5 \text{ mW/cm}^2$ have been measured under AMO test conditions at 25°C .

2.0 Introduction

The purpose of this program is to develop the necessary technology to produce very thin (0.1mm maximum), high output (17.5 mW/cm^2), silicon solar cells which will display improved radiation performance compared to present state-of-the-art devices. The major emphasis shall be in the areas of back surface field and selective etch technology. Higher resistivity (50 ohm-cm) silicon than is normally used for space flight cells will be investigated as a method for achieving the radiation objectives which are targeted as 15.5 mW/cm^2 after 3×10^{14} equivalent 1 MeV electrons/ cm^2 and 14.0 mW/cm^2 after 1×10^{15} electrons/ cm^2 .

3.0 Technical Discussion

3.1 Selectively Etched Silicon

A matrix of eighty cells composed of two surface finishes, standard chemically polished and sodium hydroxide (NaOH) etched, two resistivities, ten and two ohm-cm, and four thicknesses, 0.10mm, 0.15mm, 0.20mm and 0.25mm, was fabricated. This was done to assess the impact of NaOH texturizing on cell output as a function of bulk resistivity and cell thickness.

Cells of the required thickness were produced by two different techniques in order to achieve the desired surface finish. In the case of the standard polished surface, the cells were lapped then polished using a solution of nitric-hydrofluoric and acetic acid. The textured surface cells were obtained by initial etching in 30 percent NaOH, then final etching in a heated two percent solution of the NaOH etch.

All cells were diffused using the standard phosphine source technique and sheet resistances in the order of 90 ohms/square were obtained. This corresponds to a junction depth of $\sim .18 \mu\text{m}$ which is not optimum for either polished or textured surface cells, but it enabled us to avoid other fabrication problems which might have influenced the results.

The cells were contacted using titanium-silver evaporated through bimetallic masks to yield a configuration consisting of 9 grids/cm terminating at a 0.5mm collector bar. This yields an active area of $\sim 3.65 \text{ cm}^2$ for the $2 \times 2 \text{ cm}$ cells used based on a gridline width of $\sim 75\mu$. All these devices had a tantalum pentoxide (Ta_2O_5) antireflection coating and all test results are for unfiltered cells.

Table 1 is a comparison of polished versus textured cell electrical output for ten ohm-cm silicon as a function of thickness. Table 2 is a similar comparison for two ohm-cm silicon. All data was taken at 25°C under AMO (135.3 mW/cm^2) conditions. There are some obvious inconsistencies in this data which were caused by tooling problems and variation in the cell thickness targeted. The tooling problems caused the gridlines to vary significantly

in width, thus changing the true active area of the cell. There were additional problems with cell curve shape which caused anomalies in the reported values of maximum power. However even with these problems it is obvious that for most cases textured surface silicon solar cells yield significantly more power than cells with the standard polish-etched finish. All data was taken at 25°C under AMO (135.3 mW/cm²) conditions.

Especially in the case of the two ohm-cm data there were extremely large variations in both open circuit voltage and curve factor that resulted in polished finish cells delivering more power than textured surface cells even though the textured cells had more short circuit current. There is no absolute explanation for these results, however there is a significant amount of data from other work that indicates either a small or no difference between the two surface finishes with respect to open circuit voltage. Taken in the most optimistic light, it would appear that for thin cells, textured surfaces can yield at least ten percent more power than for polish-etched surfaces.

Table 1

Textured vs. Polished Silicon Cells (2 x 2 cm 10 ohm-cm)

Finish	Thickness (mm)	I _{sc} (mA)	V _{oc} (mV)	P _{max} (mW)
Textured	.275	154-162	555-564	66.7
Polished	.250	149-152	558-566	64.4
Textured	.20	150-153	544-551	64.4
Polished	.175-.200	138-143	557-565	59.7
Textured	.15	142-150	531-547	61.3
Polished	.15-.175	136-138	550-558	58.7
Textured	.10-.125	141-146	530-540	61.6
Polished	.10	128-130	522-537	51.8

Table 2

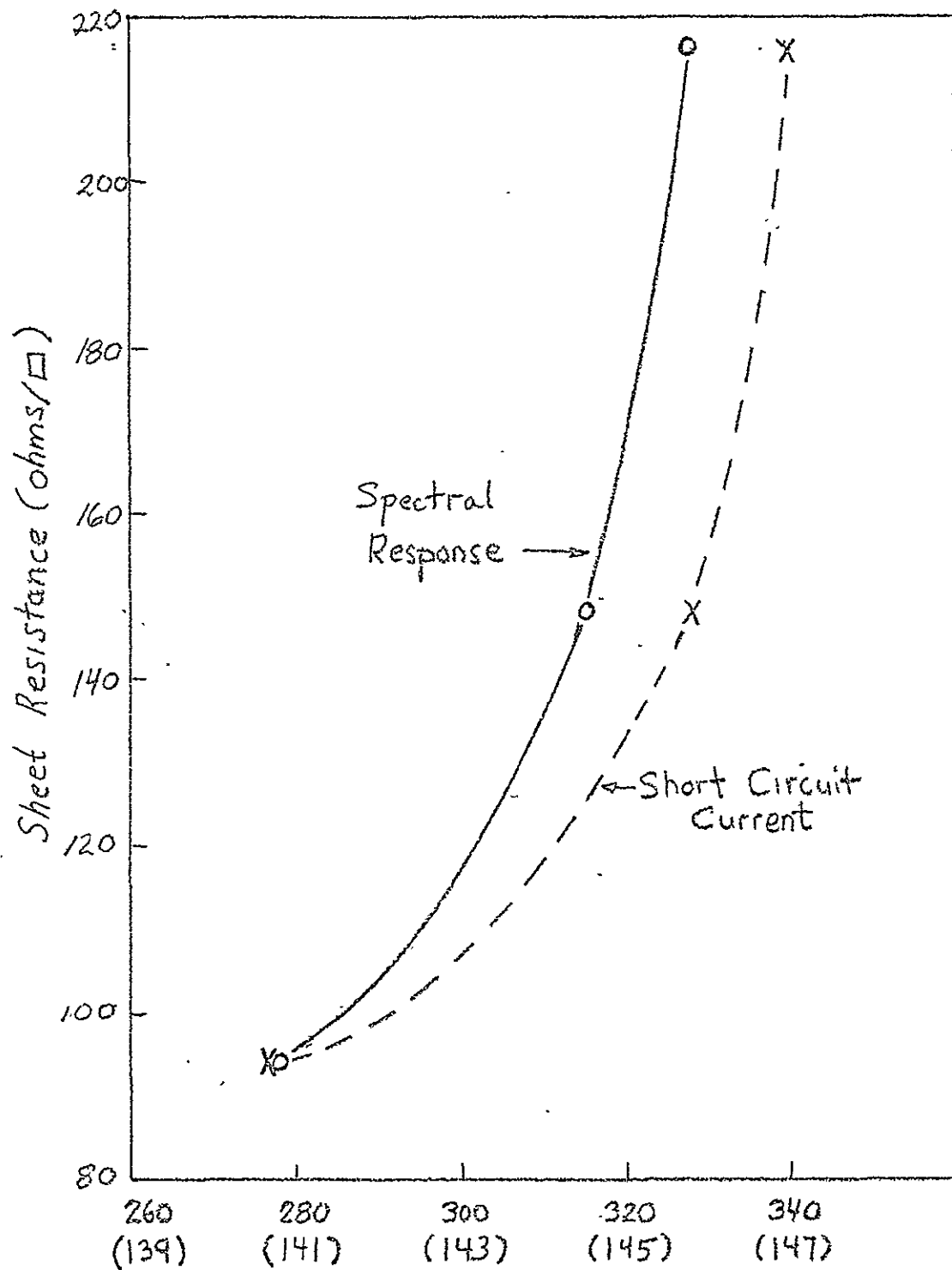
Textured vs. Polished Silicon Cells (2 x 2 cm 2 ohm-cm)

Finish	Thickness (mm)	I_{sc} (mA)	V_{oc} (mV)	P_{max} (mW)
Textured	.25	152-156	575-589	66.5
Polished	.25-.275	144-146	597-602	68.0
Textured	.225	147-152	577-583	66.6
Polished	.20-.225	143-144	592-599	67.8
Textured	.15-.175	148-152	576-584	67.5
Polished	.15	140	582-591	65.0
Textured	.075-.10	139-143	559-570	61.6
Polished	.10	132-134	569-577	59.5

3.2 Optimization of Junction Depth

Junction optimization has been done repeatedly for polish etched surface finish conditions, but relatively little data has been obtained for textured silicon cells. Ten ohm-cm, 0.225mm thick cells were used for this investigation. Diffusion times and temperatures were varied to produce cells with sheet resistances (ρ_s) ranging from 90 to 215 ohms/square. The actual sheet resistance measurements were made on polished "surrogate" wafers to avoid any anomalies that might be introduced by the saw-toothed surface. Previous studies had shown that a sheet resistance value of $\sim .125 \mu m$ was an optimum value for polished cells.

Cells were fabricated from the diffusion matrix using titanium-silver contacts. To avoid any perturbations that might be introduced by AR coating variations, the cells were not coated. The short circuit current and spectral response at 400 nm was measured as a function of sheet resistance. This data is presented in Figure 1. The results for textured surface silicon cells follows the trend previously observed for the polished surface cells, an increase in short wavelength response and short circuit current as the sheet resistance increases (junction depth decreases). This increase tends to saturate at ρ_s values of the order of 200 ohms/square. The same behavior was observed when



Spectral Response @ .4 Microns - Arbitrary Units
(Short Circuit Current - mA)

FIGURE 1

a diffusion matrix using two ohm-cm silicon was used. Since ρ_s values greater than 150-180 ohms/square require an even more sophisticated grid pattern for a relatively small increase in short circuit current ($\sim 0.25 \text{ mA/cm}^2$), it was judged that the optimized junction depth for textured cells should be targeted at $\sim 0.10\text{-}0.12\mu\text{m}$.

3.3 Fabrication of Thin (0.05mm) Cells

Since the main purpose of this program is to develop very thin silicon solar cells, preliminary work was begun to define the problem areas. For this phase, two ohm-cm textured cells fabricated by the standard techniques for manufacturing non-field, shallow junction devices were employed.

To obtain wafers in this thickness range, it was necessary to lap them to $\sim 0.25\text{-}0.30\text{mm}$, then etch to $\sim 0.10\text{mm}$ using 30 percent NaOH, and finally etch to $\sim 0.05\text{mm}$ using a heated two percent NaOH etch. This process has yielded finished $2 \times 2 \text{ cm}$ wafers ranging from 0.045 to 0.065mm (1.8-2.6 mils). Although still not completely refined, the thinning process has produced small batches of wafers with yields approaching eighty percent in some cases.

Our present evaporation tooling is not designed for extremely thin cells, therefore the contact pattern has considerable metal penumbra because the cell is not in intimate contact with the evaporation mask. This results in thin cells which have less active area than thicker $2 \times 2 \text{ cm}$ devices because of the relatively wide gridlines. The fact that the thin cell is not completely captured in the mask pocket also allows it to shift during the evaporation process. In some cases the collector bar is evaporated over the cell edge, requiring that the part be edge etched in order to remove the metal shorting path from junction to base. This is an extremely difficult process to perform when the cells are below 0.10mm in thickness because both sides must be masked, and the edges cleaned before etching. The yield from this process is extremely low (less than twenty percent) due to breakage from excessive handling.

Another noticeable problem with very thin cells is the mechanical effect of the contacts. The mismatch in the thermal coefficients of expansion between the silicon and the contact metals produces a significant amount of cell bowing. Since the back of the cell is fully covered with metal, while only ~ 8 percent of the front is covered, the difference leads to a net stress effect from the back contact metal. This has made us think about

the possibility of using a grid pattern for the back contact, when very thin back surface field cells are produced. The back surface field cell has an effective sheet resistance on the order of 35-40 ohms/square and therefore it may be possible to consider a grid pattern, perhaps in conjunction with a small contact pad, as a back contact.

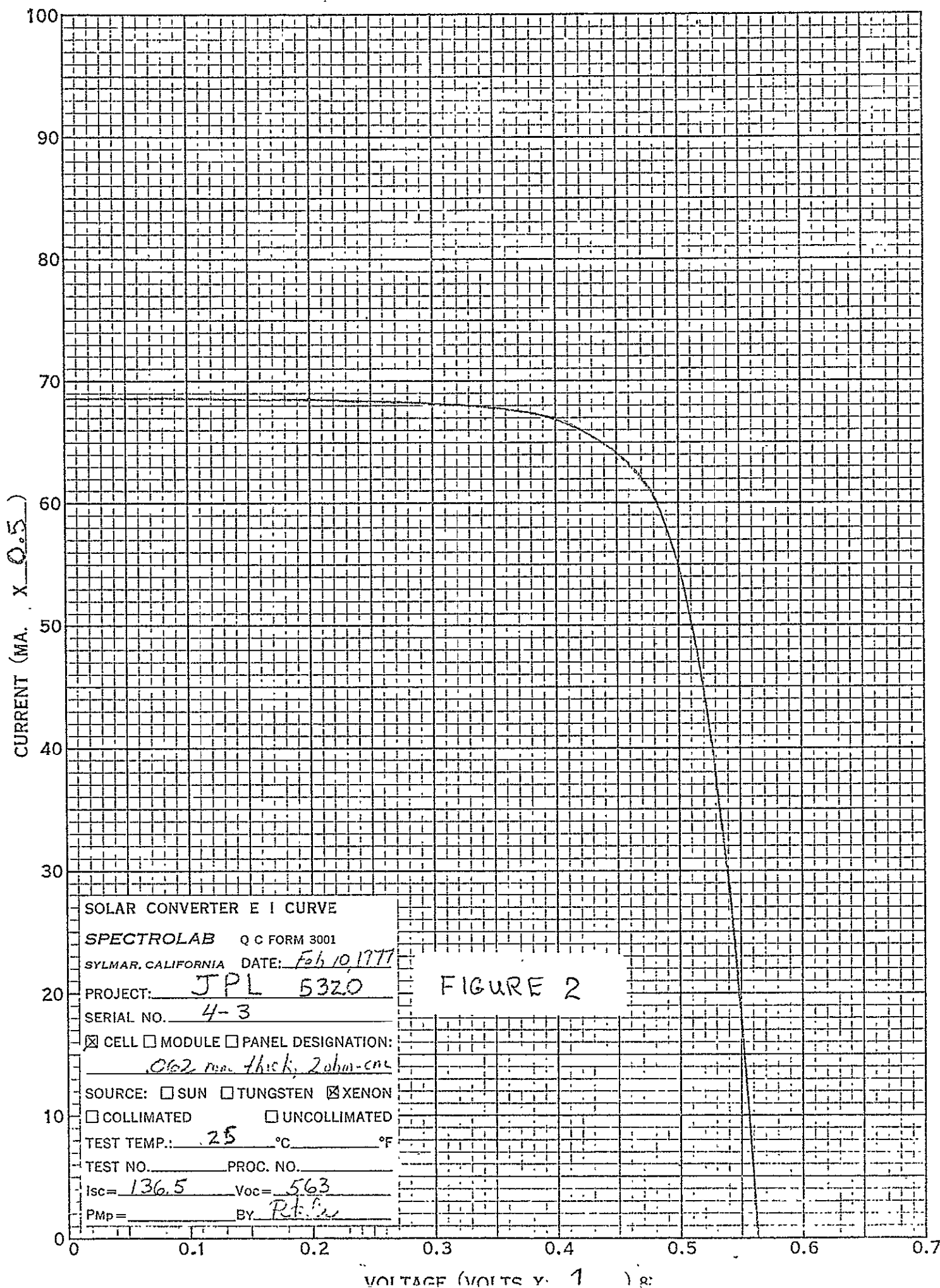
To date approximately fifty 2 x 2 cm cells have been completed that have an average thickness of .060mm as determined by cell weight. This method of determining cell thickness, has been used because the cell's surface is composed of tetrahedrons and the standard micrometer reading thus gives only the high spot (tip of the tetrahedrons) on each side of the cell. Since the average height of the tetrahedrons is estimated to be $\sim 6 \mu\text{m}$, this will introduce a systematic error of $\sim 12 \mu\text{m}$ (two sides) which is significant when the total cell thickness is in the order of 50 μm . In addition it has been our experience that the textured surface is relatively sensitive to handling and use of a micrometer may create damage to the surface.

Although these very thin cells show a wide spread in output, reflecting many of the problems expressed in the previous paragraphs, the better cells have shown $\sim 58 \text{ mW}$ when measured under AMO conditions at 25°C . An I-V curve of one of these is shown in Figure 2.

A preliminary analysis of our processing shows that the major causes of thin cell breakage are from 1) bulk finishing, where the normal wafer specification for taper of .025mm can lead to extremely thin localized areas in the wafer, 2) back etching, where the masking, etching and cleaning steps require a great deal of cell handling and 3) cell contacting, where the cells are required to be placed in close fitting metal frames which can cause edge and corner chipping. As mentioned before, cell bowing caused by the back contact metallization is another significant cause for concern.

3.4 Back Surface Field Optimization

Almost all back surface field (BSF) processing technology has used evaporated aluminum as the acceptor source for forming the back surface region in silicon. Although excellent results have been achieved using evaporated aluminum sources, the process has never been completely understood or controlled. Experimental work has shown that the effectiveness of the BSF is a function of the amount of aluminum used as the source, increased amounts of aluminum yield cells with higher open circuit voltages and short circuit currents. It appears that a minimum of 4 μm of aluminum source is necessary in order to obtain an optimized BSF effect.



Another important set of parameters that appear to control this effect are the time and temperature which are used to drive the aluminum into the silicon. It has been our experience that temperatures in the order of 800°C and higher coupled with heating times of between fifteen and thirty minutes are necessary. This observation has created problems since it is desirable that the BSF effect be coupled with a shallow junction in order to obtain the maximum power output from the cell. This need prevents a simultaneous process that provides both the optimum BSF effect and an optimized shallow junction. A simultaneous processing step limits the junction depth to .18µm and greater.

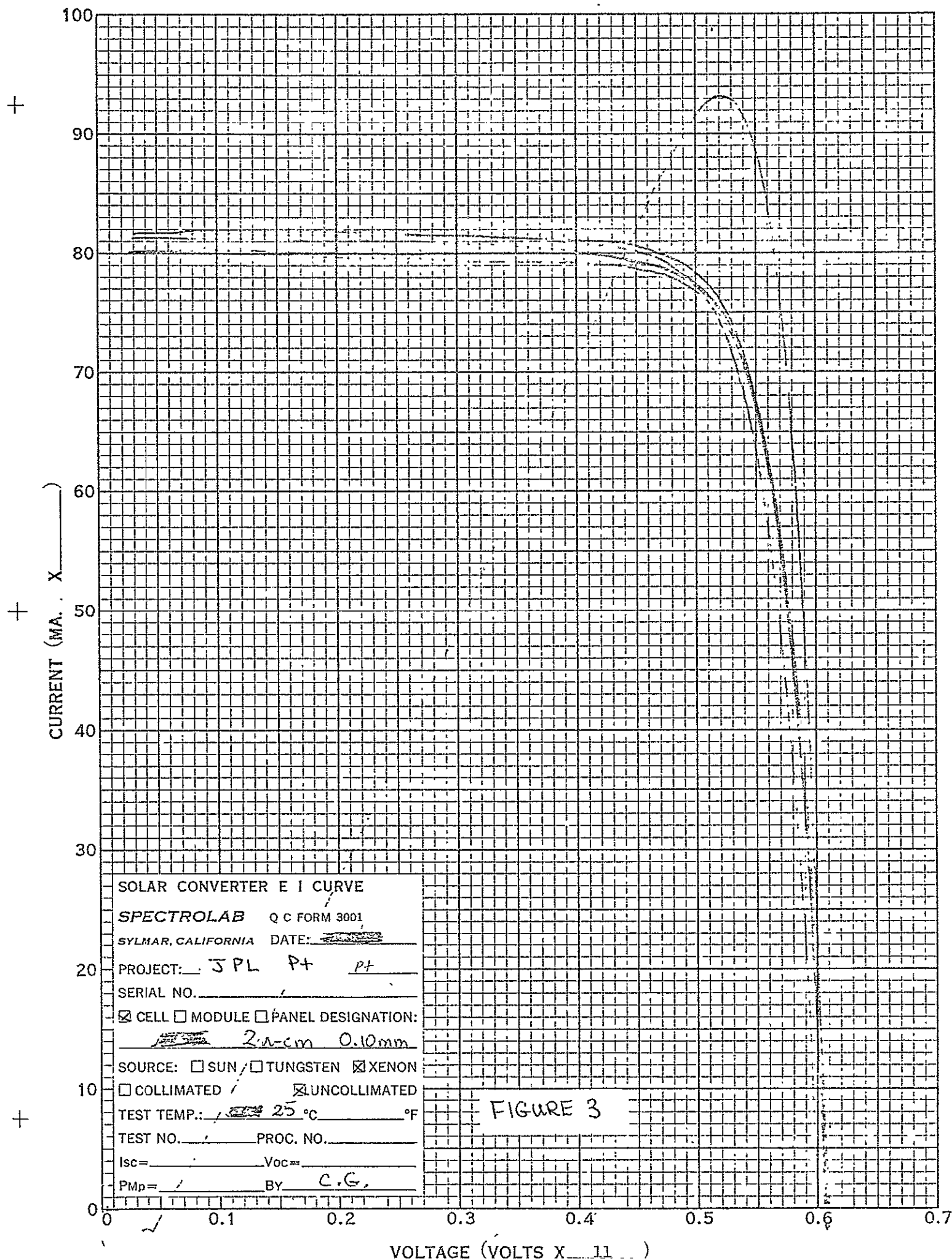
Therefore efforts aimed at developing a two step process (field formation, then junction formation) were instituted. It was found that the phosphorous source would compensate the acceptor doped field region thus reducing the BSF effect. The alternate approach, junction formation followed by field formation, was investigated under this contract. A group of silicon wafers were phosphorous diffused to form a shallow junction (0.1µm), then the cells were separated into subgroups for field formation. The purpose of this approach was to see if a very short time at a relatively high temperature could create a useful BSF effect without driving the deposited phosphorous region further into the silicon. Temperatures as high as 900°C were investigated. Times were varied from 30 seconds to 2 minutes for temperatures of 875 and 900°C. In order to expedite this investigation the wafers were evaluated at this point by means of probe measurements of the cell voltage under AMO illumination. An optimized BSF process will show an open circuit voltage of between 580 and 600 mV for an operating temperature of 25°C using this technique. Regardless of the firing schedule chosen, the best open circuit voltages measured were between 560 and 570 mV.

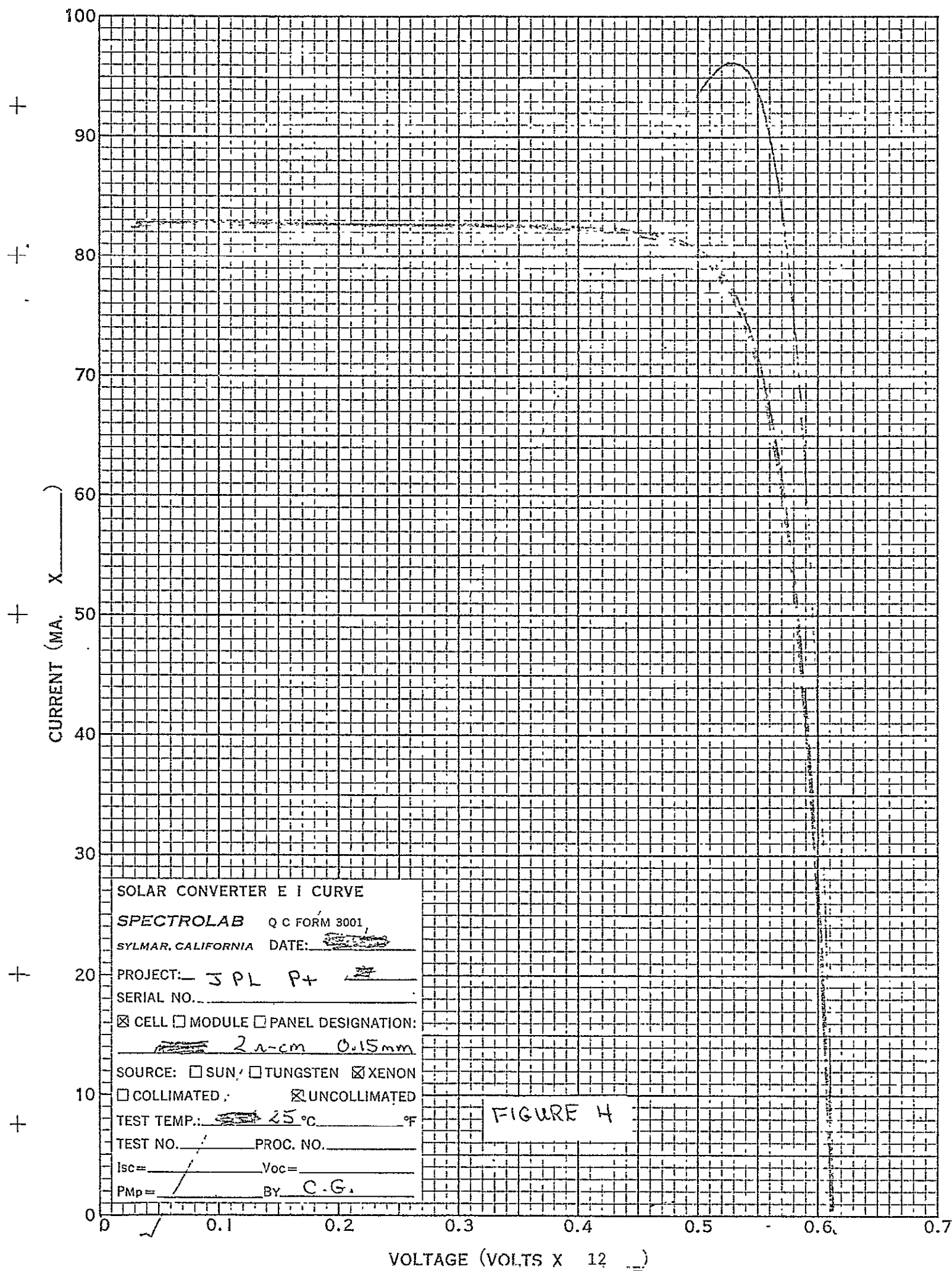
In parallel with this effort, an investigation of an organic based aluminum paste source was undertaken. The stimulus for this was derived from a NASA-Lewis funded program in which the aluminum paste had been successfully employed to produce BSF cells with open circuit voltages as high as 600 mV for .020mm, 10 ohm-cm base material. The paste is applied to the wafer using screen printing, and by controlling the screen mesh size and the emulsion thickness, it is possible to print relatively thin layers (25µm) of paste. Since the

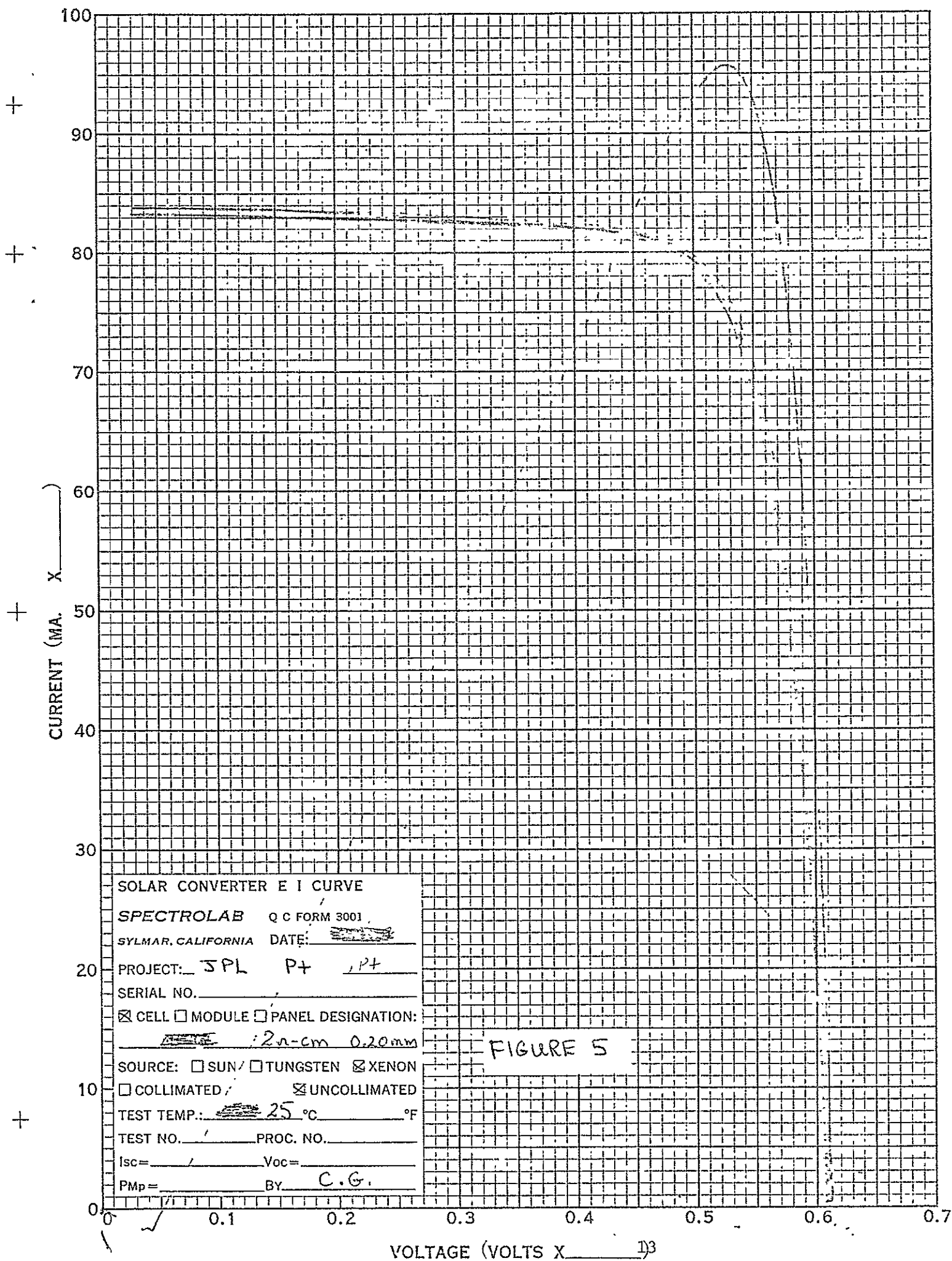
aluminum comprises more than one-half the paste thickness, it is equivalent to depositing more than 12 μm of aluminum, well above the minimum required for an optimized field effect.

After printing the paste, the organic binder is driven off by air baking, leaving a layer of aluminum consisting of very small individual particles, a few microns in diameter. It was found that this type of aluminum source could produce an effective BSF when heated to temperatures in excess of 750°C for periods of one or two minutes. Since this did not have a significant influence on the junction depth, this process is being employed to produce shallow junction BSF cells. In brief it consists of forming a shallow junction ($0.10\text{--}0.12\mu\text{m}$) using a phosphine diffusion, then removing the junction from the back surface by etching. Then the aluminum paste is screen printed on the etched surface, fired to drive off the binder and and fired for one or two minutes at a temperature greater than 750°C to form the field region. This technique has been successfully employed to produce BSF cells as thin as 0.1mm . Below this cell thickness, severe warping of the silicon due to the difference in expansion properties between it and the aluminum leads to cell breakage. It may be possible to modify the printing process to produce thinner paste layers and thus allow silicon blanks 0.05mm thick to be fabricated into cells. Attempts to extend this technology to even thinner cells will be made during the next few months.

Work has begun on producing the BSF matrix using this process. Cells ranging in thickness from 0.1 to 0.25mm with resistivities of nominal two, ten and one hundred ohm-cm are to be fabricated. Table 2 is a summary of the electrical characteristics of the cells made to date. Figures 3, 4, 5 and 6 show I-V curves for the best cells from each 2 ohm-cm element of this matrix. There have been some problems in obtaining high resistivity silicon, and until this is resolved, the matrix cannot be finished. In the event that one hundred ohm-cm material cannot be obtained in a timely fashion, we would propose to substitute nominal 50 ohm-cm material, which is available.







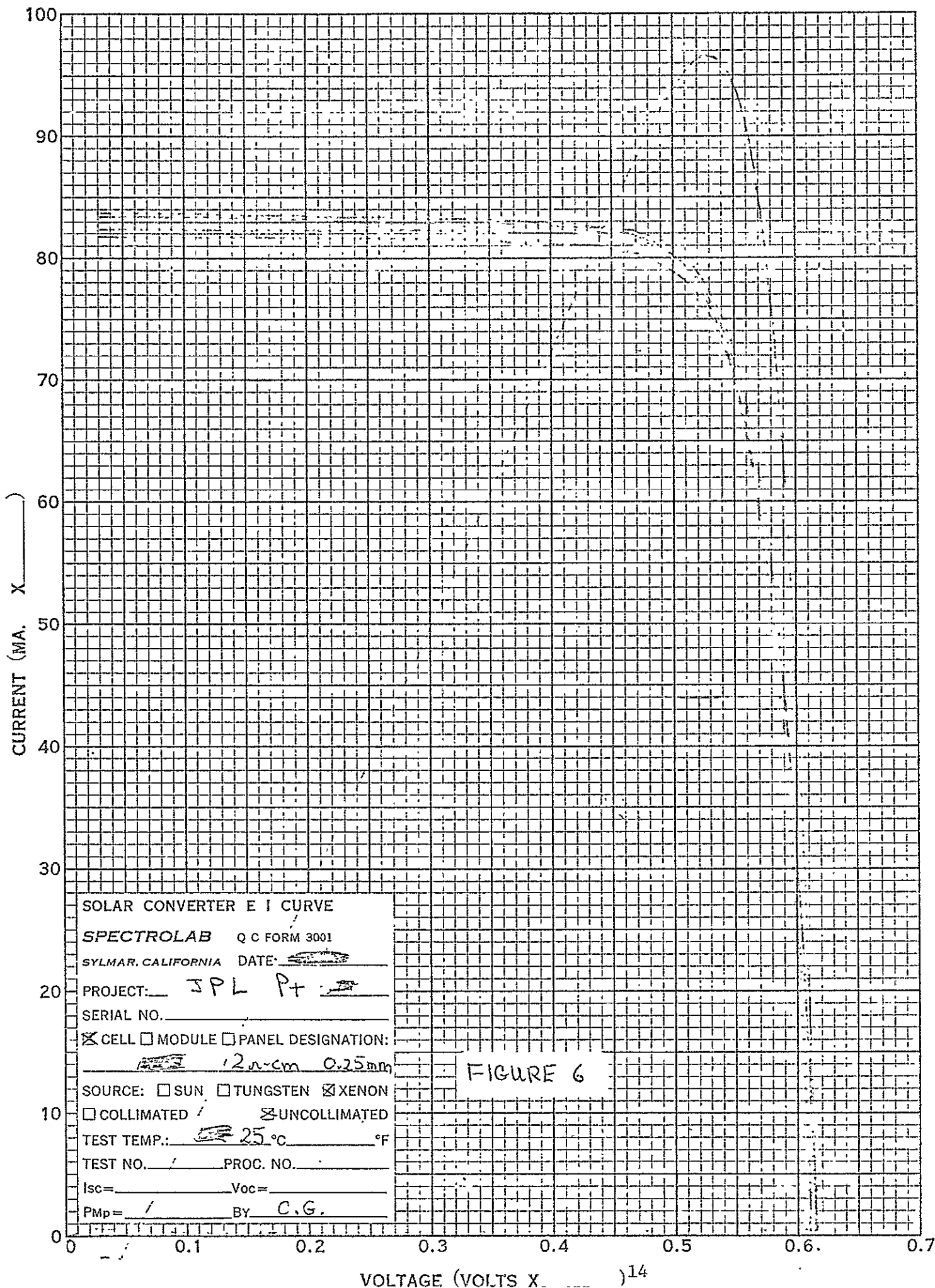


Table 2

Electrical Characteristics of 2 x 2 cm BSF
Silicon Solar Cells (25°C)

Resistivity (ohm-cm)	Thickness (mm)	$\bar{I}_{sc}$ (mA)	$\bar{V}_{oc}$ (mV)	FF	$\bar{P}_{max}$ (mW)
2	0.10	162	608	.79	78.0
2	0.15	165	612	.80	81.1
2	0.20	167	611	.79	80.3
2	0.25	166	613	.79	80.8
10	0.10	162	602	.795	77.7
10	0.20	169	605	.775	79.3
100	0.10	165	605	.78	77.9
100	0.20	170	598	.76	77.5

4.0 Conclusions

An optimized process for fabricating textured surface, BSF cells as thin as 0.10mm has been developed. The key to this process is the development of an aluminum paste source which is capable of producing an optimized BSF effect in a reliable reproducible manner. Conventional technology can be used to produce textured surface 0.05mm thick cells with the potential for a mechanical yield in excess of fifty percent. It is not known if the BSF paste process can be extended to silicon less than 0.10mm thick. Based on our work to date it seems feasible to project that 0.10mm cells having AMO efficiencies of fourteen percent can be produced in volume with an acceptable yield. It may be possible to produce 0.05mm cells with AMO efficiencies approaching twelve percent without using BSF technology and if a method of incorporating this effect into 0.05mm cells can be found it may be possible to obtain AMO efficiencies of thirteen percent.

5.0 Recommendations

Spectrolab recommends that all future work now concentrate on silicon less than or equal to 0.15mm in thickness. In the event that BSF technology cannot be applied to silicon less than 0.10mm in thickness, we would suggest investigating the use of a back reflector in an effort to increase output power in cells 0.05mm thick. In view of the delivery requirements over the next two months we feel that it is important that efforts to implement the concept of the border reinforced 0.025mm silicon blank be started immediately.

6.0 New Technology

Spectrolab has no new technology to report at this time. The paste aluminum BSF process was developed on contract NAS3-20029 and was reported as new technology for that program.

7.0 Projected Work - Next Three Months

The BSF matrix cell group will be completed and delivered to JPL for evaluation. Work will begin on the optimized cell matrix consisting of 0.10 and 0.15mm thick cells. Efforts to optimize 0.05mm cell output using either BSF and/or back reflector technology will begin in order to meet the delivery schedule for 200 0.05mm optimized cells as well as 100 textured surface cells of that thickness.

8.0 Projected Work - Next Six Months

Efforts will concentrate on producing 0.025mm blanks for delivery and the assessment phase of this program will be finished.